Bias-T Inductor Design support Tool

Operation Manual

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Murata Manufacturing Co., Ltd.

Tool Overview

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Find optimal products combination for PoC bias-T inductors by simple operations.

Operations

- setting conditions (circuit, criteria, current, cable (In case selected "with cable "))
- pressing the Optimize button to discover

Select circuits and criteria
Input current value
Input cable type and length (only when with cable)

Result

- optimal products combination
- the graph display of S21 (IL), S11 (RL), S21/S11, Z
- Pass/Fail for standards that are to be cleared
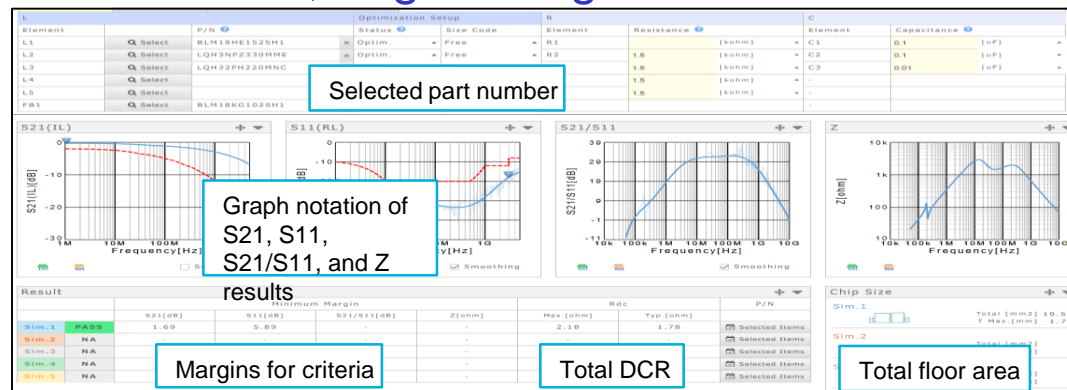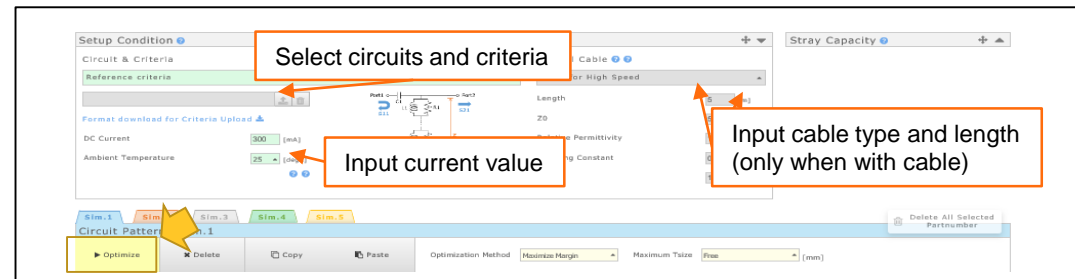- the smallest margin, total DCR/area of filters, largest height

Selected part number
Graph notation of S21, S11, S21/S11, and Z results
Margins for criteria
Total DCR
Total floor area

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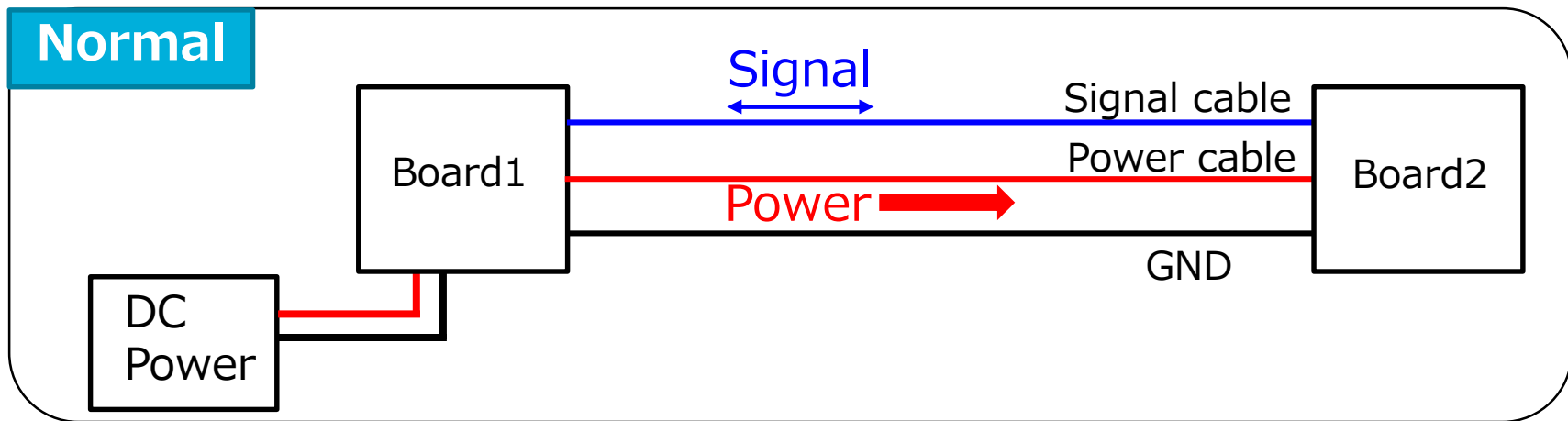
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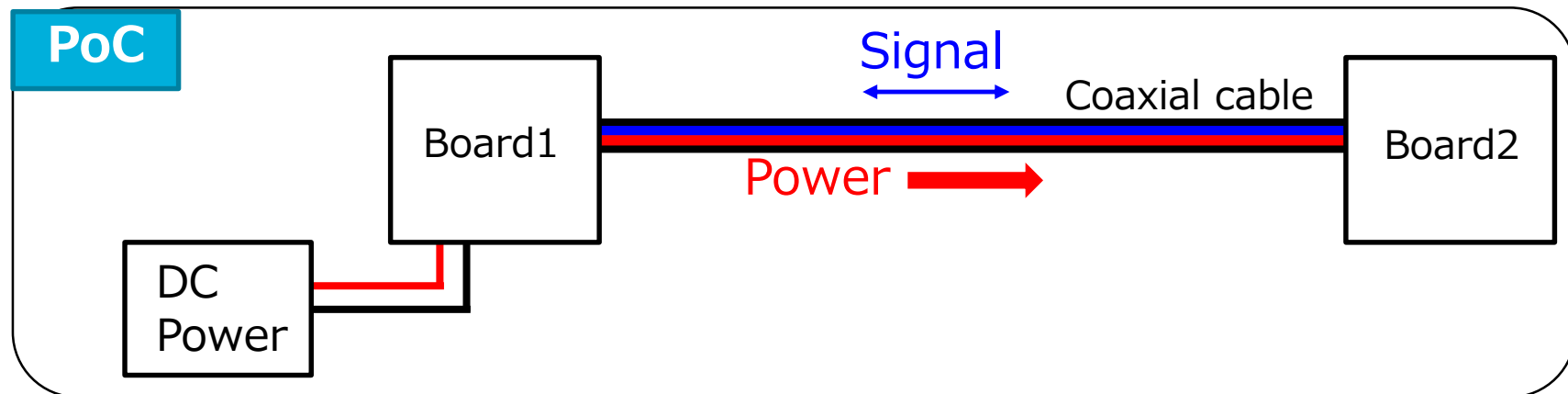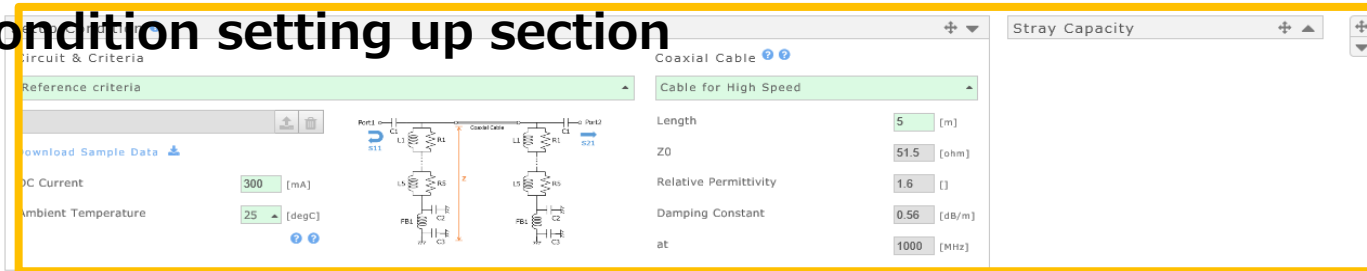
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1-1, What Is PoC

Normal

Signal

Signal cable

Power cable

Board1 — Board2

Power

GND

DC Power

PoC

Signal

Coaxial cable

Board1 — Board2

Power

DC Power
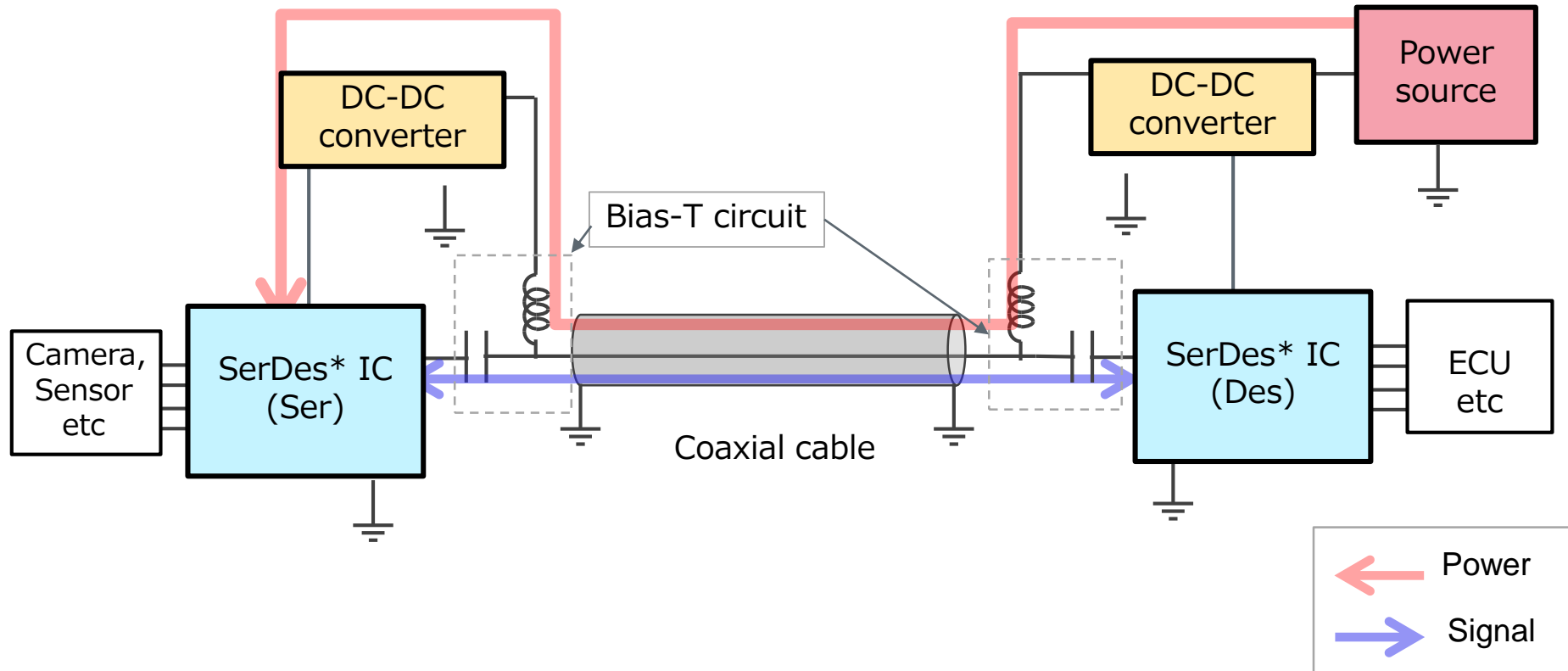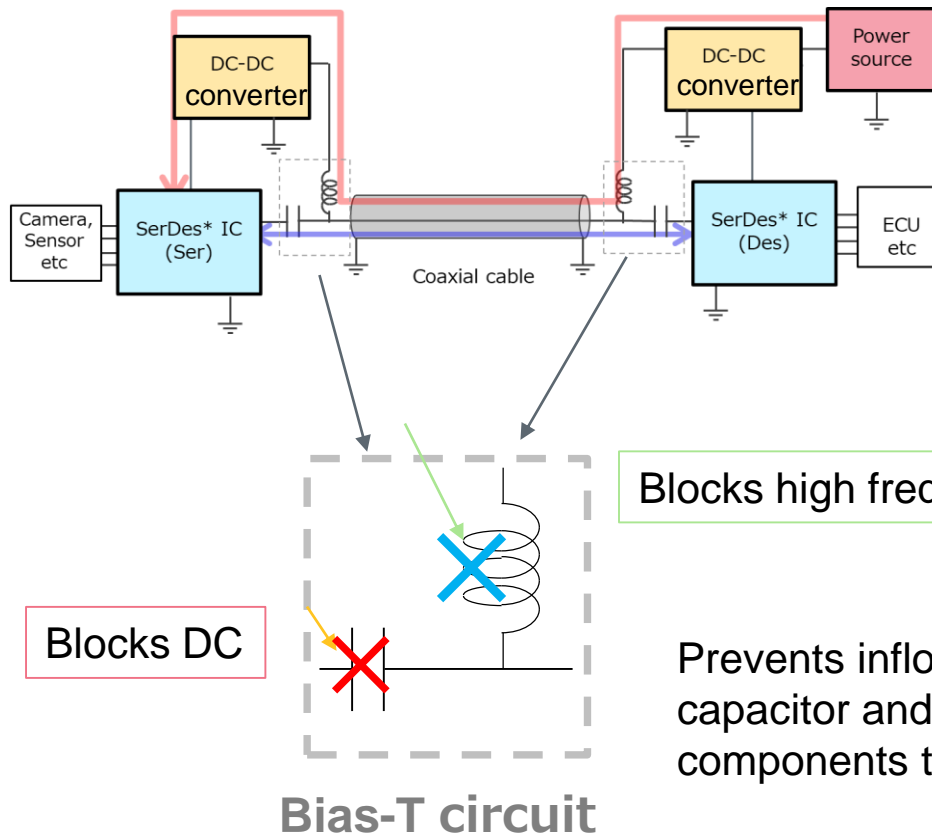
PoC (power over Coax) is a technology that transmits both power and signal simultaneously through 1 coaxial cable. (This contributes to reduce the number of cables)

1-2, Typical Circuit Diagram of PoC Systems

The high frequency signal and DC power are separated through the Bias-T circuit.
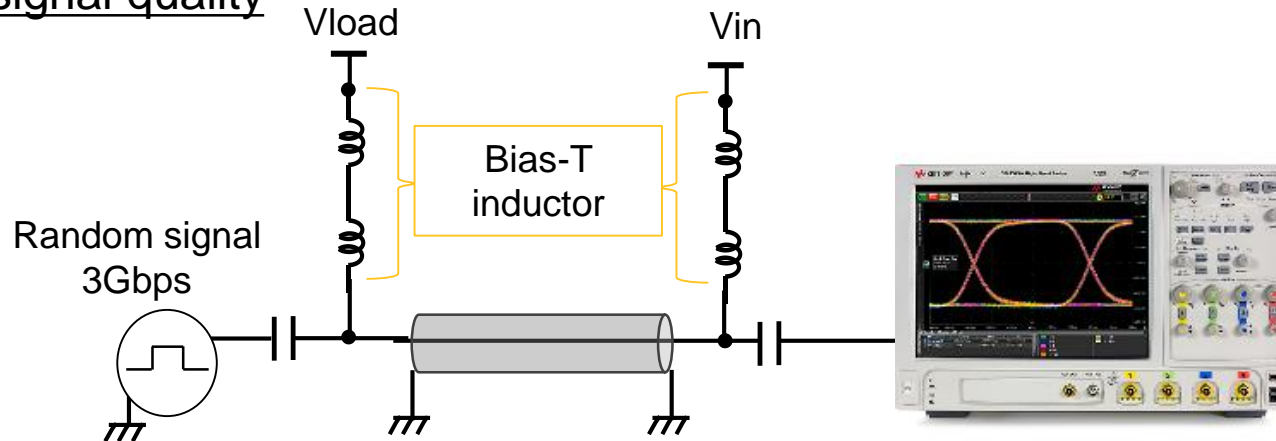
1-3, Roles of PoC System Bias-T Inductors

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Blocks high frequencies

Blocks DC

Bias-T circuit

Prevents inflow of DC components to the IC with the capacitor and prevents inflow of high frequency components to the power line with the inductor.

It is particularly necessary to select a Bias-T inductor since it greatly affects transmission characteristics.

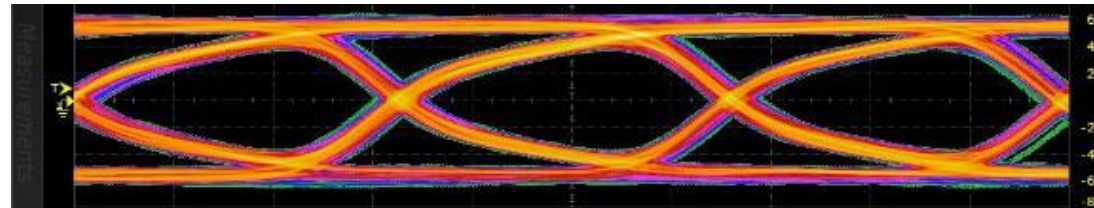# 1-4, Effects Bias-T Inductor Characteristics Apply on Signal Quality

Measuring signal quality

Vload   Vin

Bias-T inductor

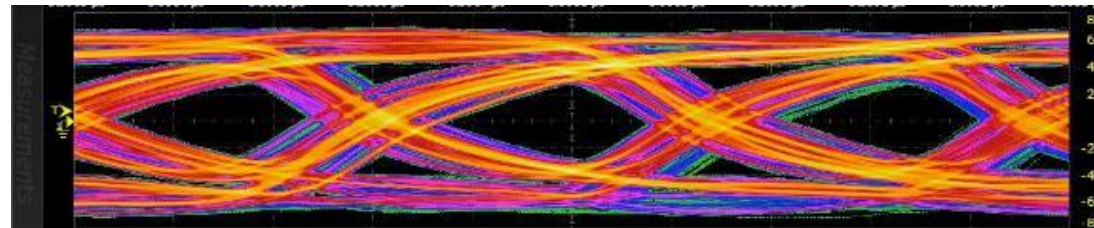Random signal 3Gbps

Bias-T inductor with good characteristics

Bias-T inductor with insufficient characteristics

It is required to select a Bias-T inductor that can ensure signal quality.

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2-1, Circuits That Can Be Simulated

Simulation with 3 types of circuits available.

Coaxial cable
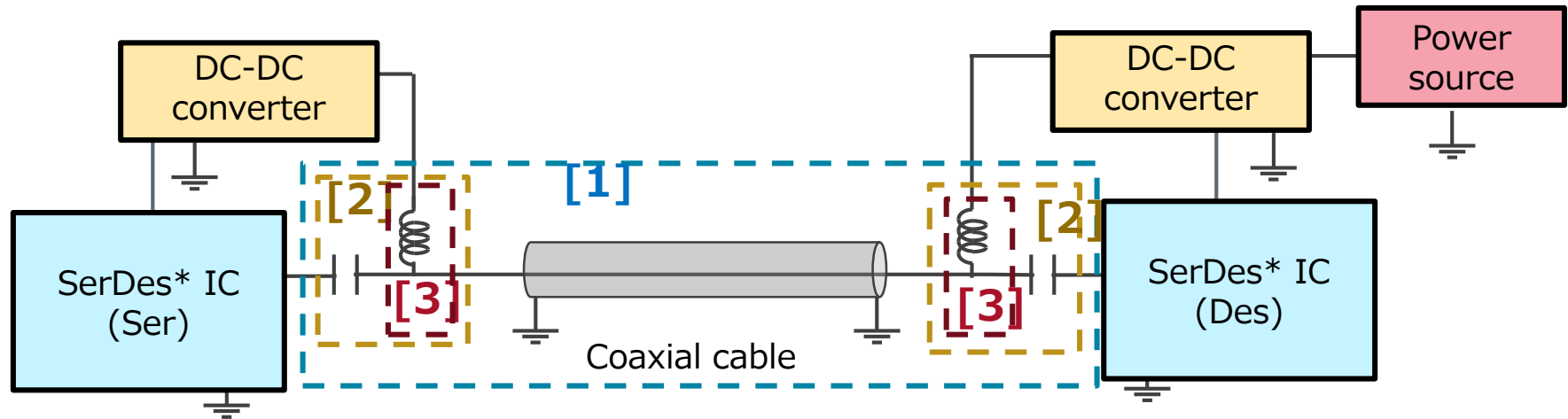
[1] With cable   [2] Without cable   [3] Only circuit

10
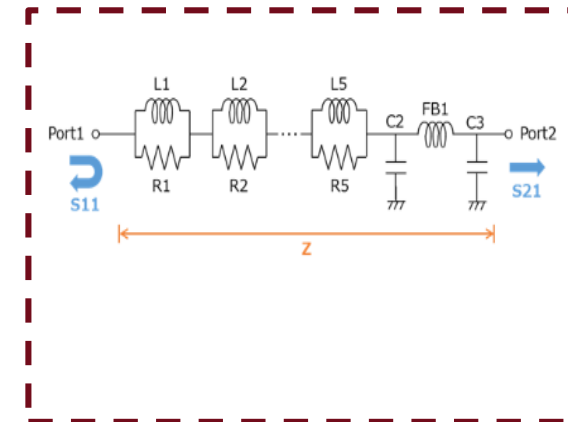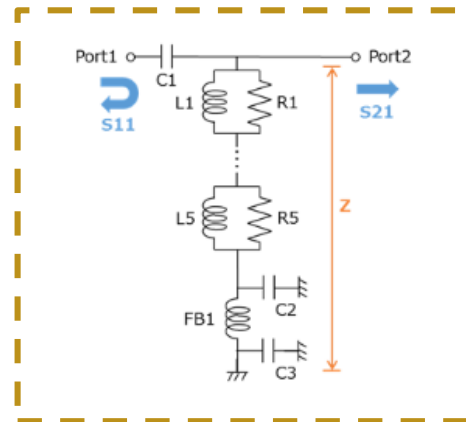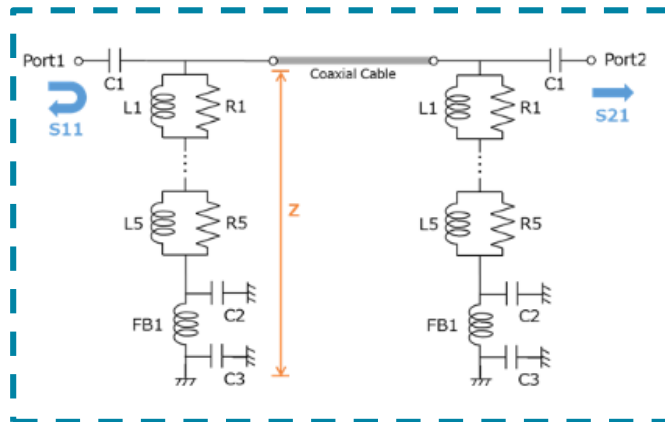
2-2, Criteria

S21, S11, S21/S11 criteria values that must be cleared to ensure signal quality are set by each IC manufacturers or customers.

Automatically selects products combinations that clear these criteria.

This tool can be selected from the following.

- Select the IC manufacturer recommended criteria
- Select the criteria set by MURATA
- Upload your criteria

2-3, Coaxial Cable

Loss varies by cable type and length.
To run simulations on circuits with cables, settings considering cable characteristics must be applied.

Relationship between cable length and S-parameter
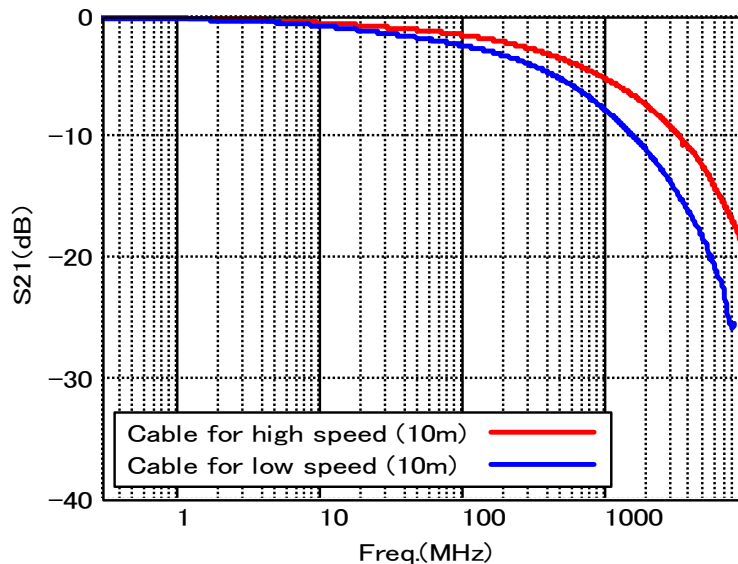
2 types of cables can be selected on this simulator.
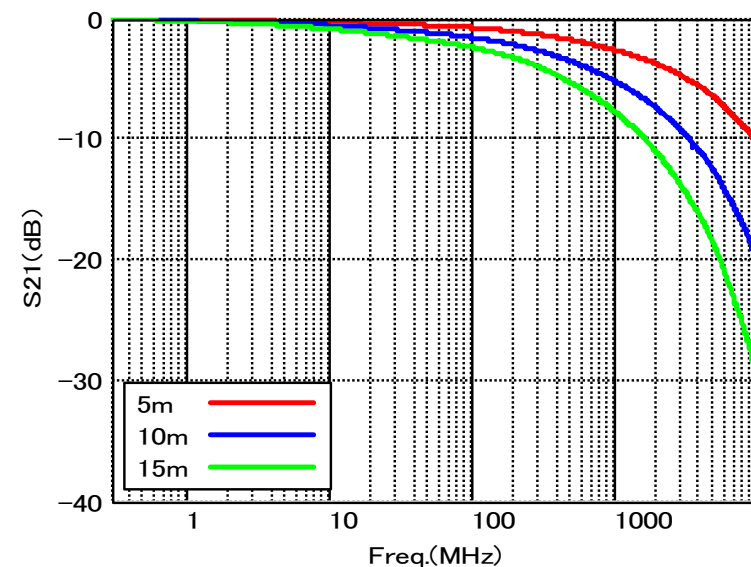
Input an applicable value for cable length.
(Usually about 15 m or less)

2-4, Current, Temperature, and Size Settings

Inductors that match the conditions set in condition settings are provided.
Applying less options for ambient temperature conditions and current conditions provide more inductors that can be selected.

2-5, Serial Connection of Bias-T Inductors

In Bias-T circuits, to ensure signal quality by reducing loss in wide bandwidths ranging from low frequencies to high frequencies, **Multiple inductors must be used in series.**

Good characteristics by connecting
Large L inductors＋Medium L inductors＋Ferrite beads

Loss in wide bandwidths can be reduced by combining the following:
- Large L inductors that cover low frequencies
- Medium L inductors that cover intermediate frequencies
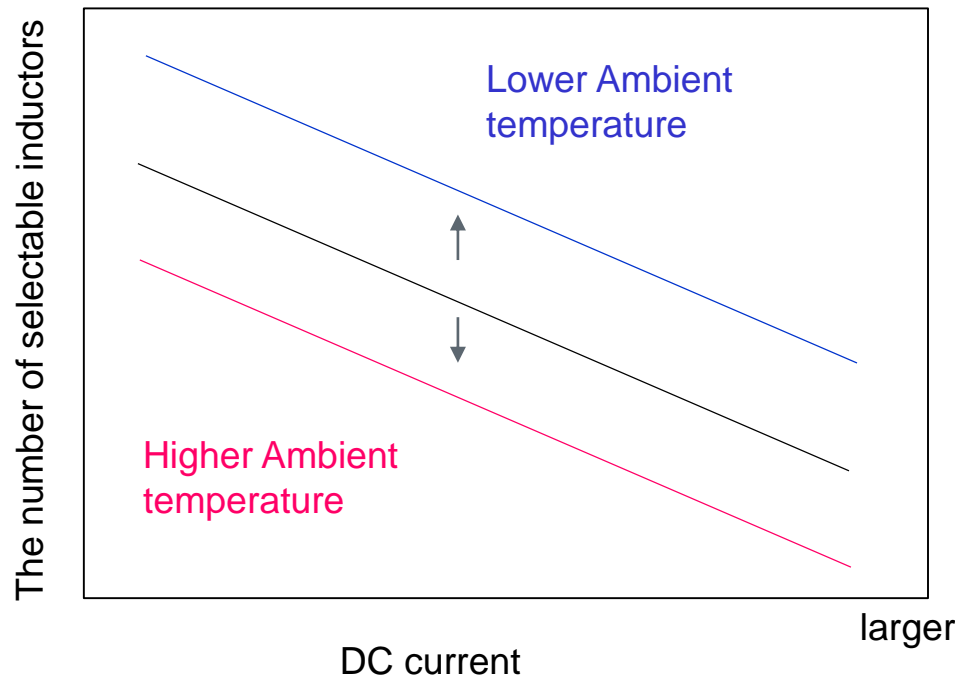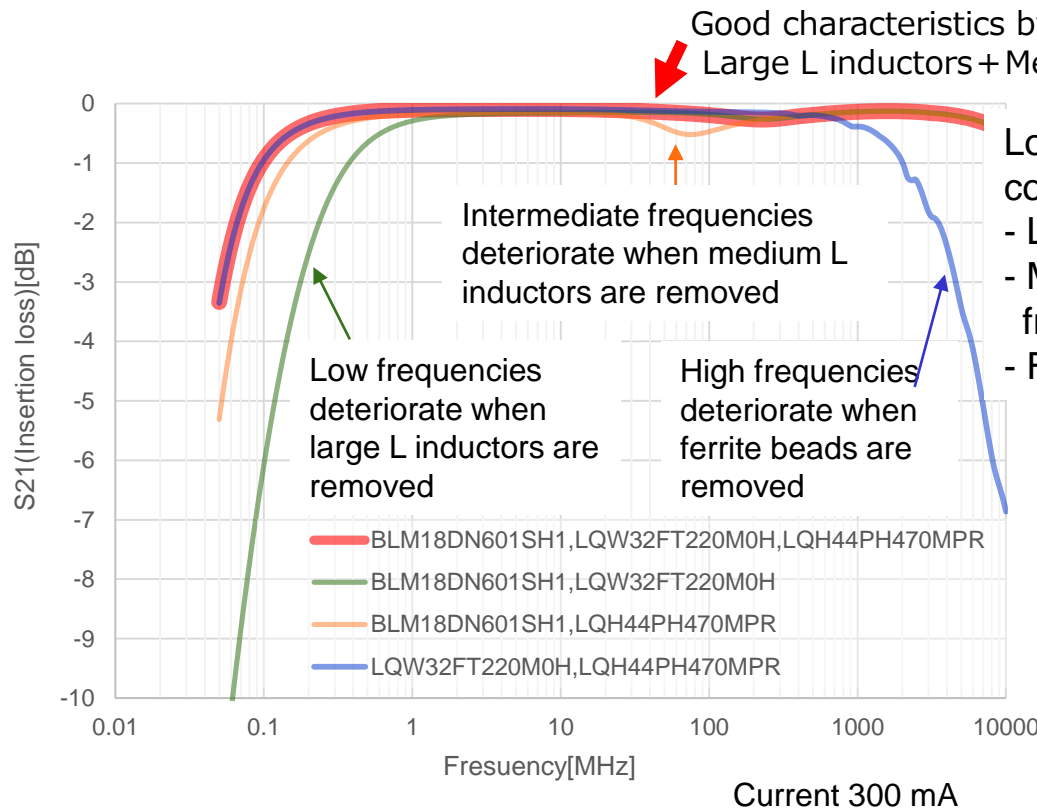- Ferrite beads that cover high frequencies

Intermediate frequencies deteriorate when medium L inductors are removed

Low frequencies deteriorate when large L inductors are removed

High frequencies deteriorate when ferrite beads are removed

BLM18DN601SH1,LQW32FT220M0H,LQH44PH470MPR
BLM18DN601SH1,LQW32FT220M0H
BLM18DN601SH1,LQH44PH470MPR
LQW32FT220M0H,LQH44PH470MPR

S21(Insertion loss)[dB]
Fresuency[MHz]
Current 300 mA

Port1 C1 L1 R1 S11 L2 R2 Z L5 R5 Port2 S21

Simulations with up to 5 parallelly connected inductors are available on this tool.
Bias-T inductors are automatically selected.

2-6, How to Select Parallel Resistances

Anti-resonance will occur when several Bias-T inductors are connected serially. **By adding a parallel resistance to each inductor, anti-resonance can be suppressed.**
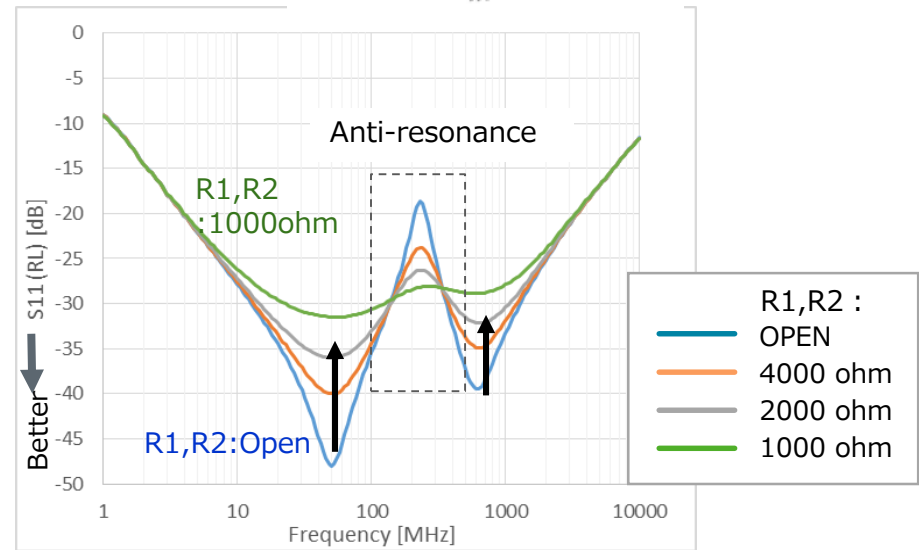
On the other hand, **characteristics other than anti-resonance will deteriorate. By selecting a suitable resistance value, a filter characteristic that fulfills the target characteristic will be achieved**.

The following are results when "L1: LQW18CNR47" and "L2: LQW32FT100" are used, and their parallel resistances R1 and R2 are Open, 1000 ohm, 2000 ohm, or 4000 ohm.
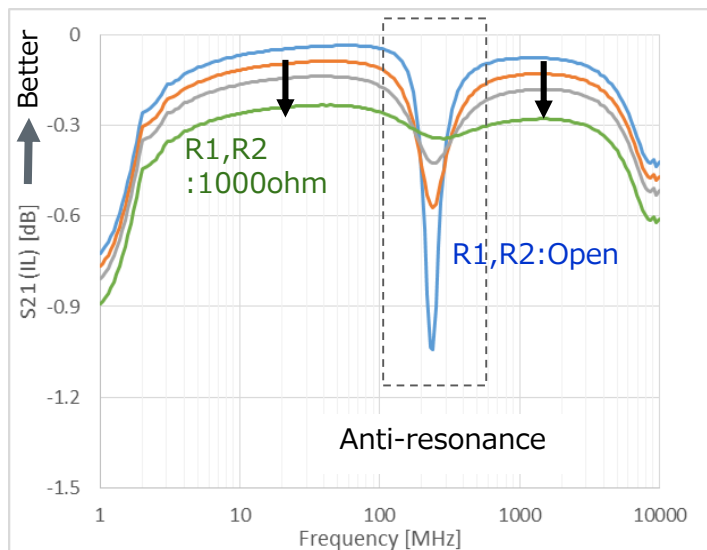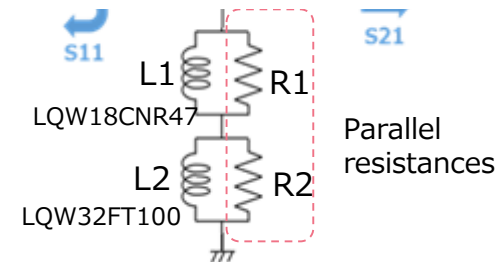
2-7, Effects of Board Stray Capacitance 1

A difference in characteristic results occurs between the simulation value (ideal state) and actual value (board implementation).
Anti-resonance is present more noticeably in the actual value.

Simulation value vs. Actual value
(ideal state)   (board implementation))
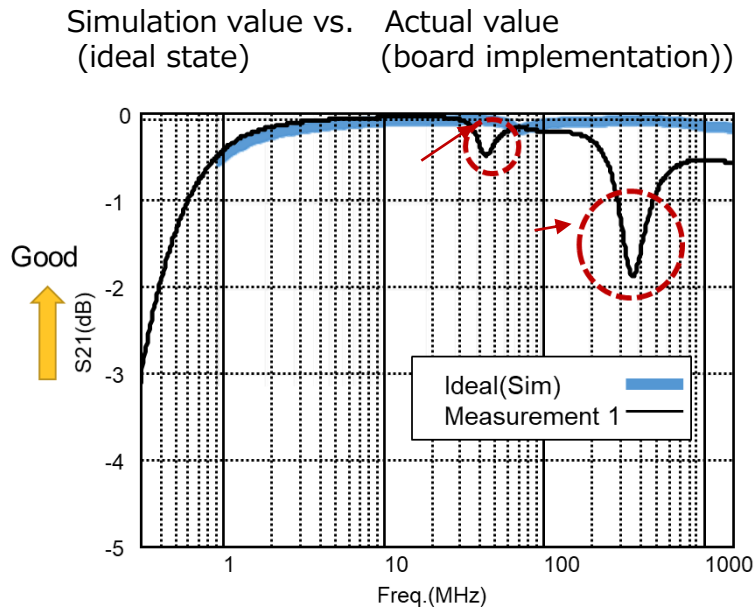
Actual board layout and measurement state

Layout of each layer

Port1   Port2

Cupper (GND)   Cupper (GND)

DC port
Upper layer   Inner layer   Bottom layer

Cross-section

Inductor
Upper
Inner   ← FR4
Bottom

Measurement state

0.033uF
Port1   Port2
L1: LQW18CNR12
L2: LQW32FT3R3
L3: LQW32FT3R3
L4: LQH3NPZ6R8
0.01uF
0.1uF

2-7, Effects of Board Stray Capacitance 1

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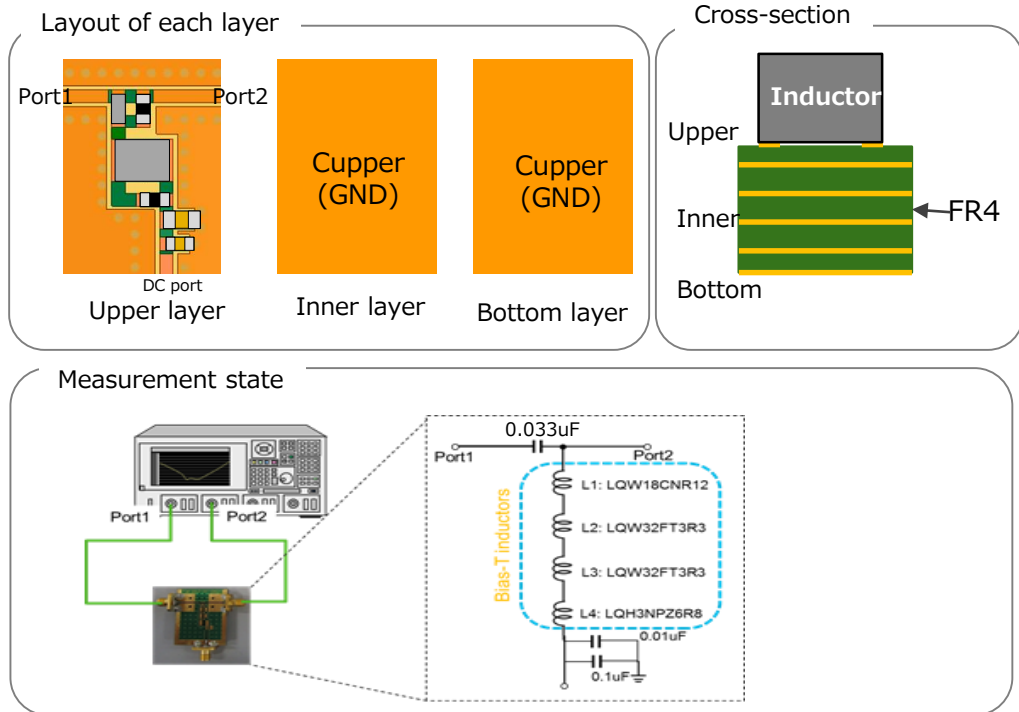
In the actual state, the stray capacitance that occurs between the inductor and inner layer of PCB is present on the characteristic.

If simulations are performed considering the stray capacitance, the calculated value becomes closer to the actual value.
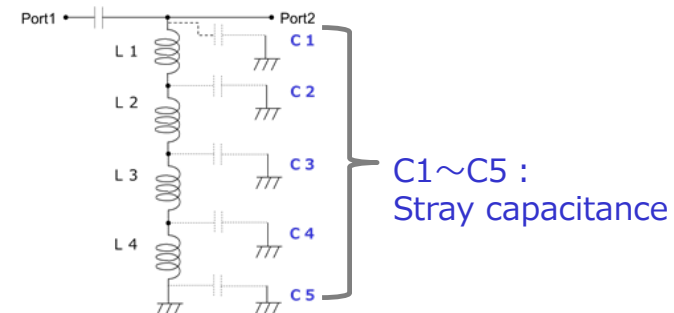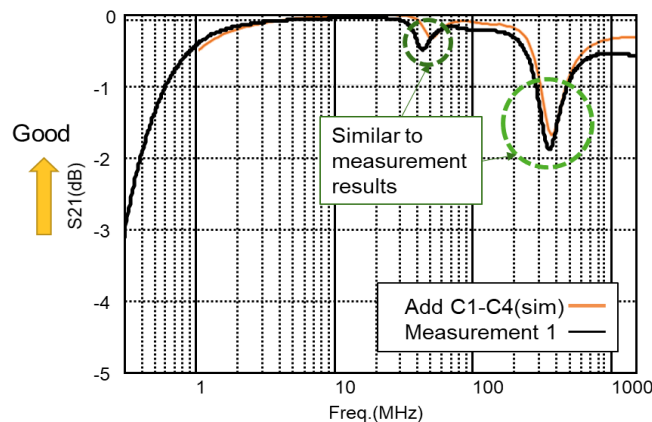
Inductor

Stray capacitance

Layer-to-layer thickness of boards d = 0.2mm

Permittivity of boards ε_r=4.5
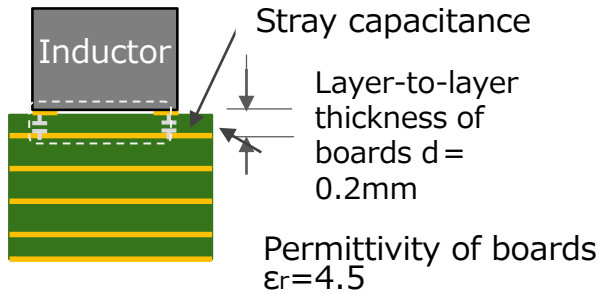
Calculating the stray capacitance from the part size and board information.
$[C=\varepsilon \times S/d]$ (S: area)

In this case

C1	C2	C3	C4
0.25pF	1.6pF	1.6pF	1.8pF

Reflected on the simulation

Simulation value (including stray capacitance) versus actual value (board implementation)

Good

S21(dB)

Similar to measurement results

Add C1-C4(sim)
Measurement 1

Freq.(MHz)

Port1　Port2
L 1　C 1
L 2　C 2
L 3　C 3
L 4　C 4
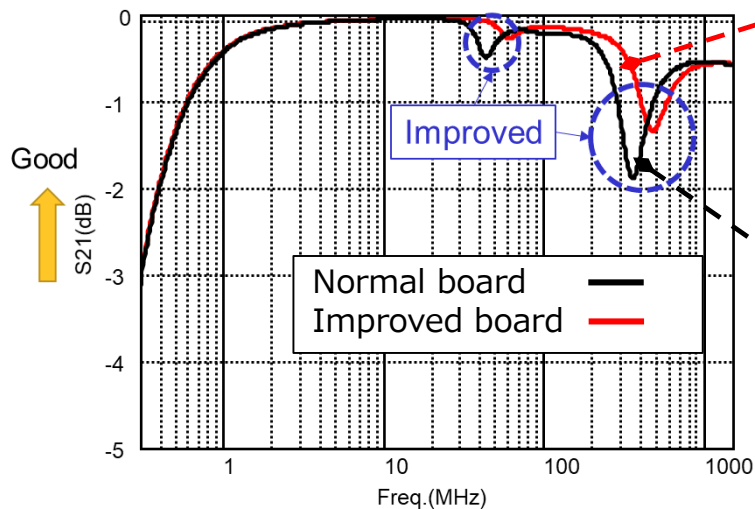　　　C 5

C1～C5 :
Stray capacitance

This simulator enables stray capacitance setting that allows calculation of results close to the actual characteristic.
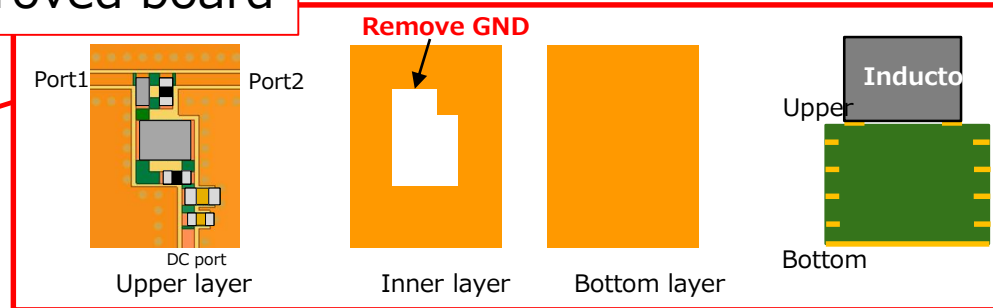
2-7, Effects of Board Stray Capacitance 2

The smaller stray capacitance is, anti-resonance becomes smaller as well.
Deleting the interior ground of the board suppresses anti-resonance.
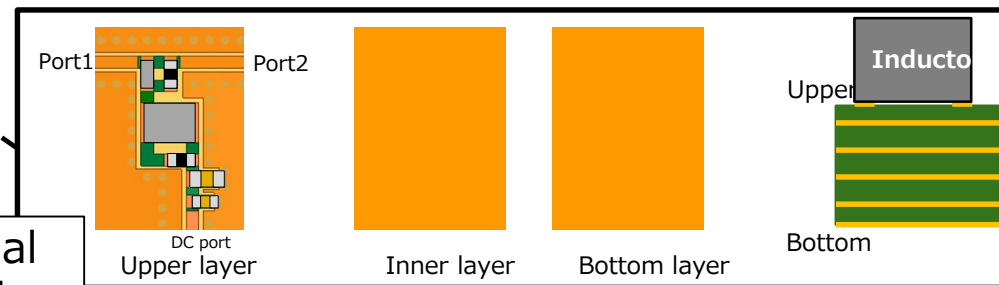
Normal board (actual measurement) versus improved board (actual measurement)

The stray capacitance value of the improved board is set as the default value on this simulator. Since the values change depending on the part size and board characteristics, simulations can be performed with the users freely changing the values.

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3-1, User Interface

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Condition setting up section

Each elements setting and selected part number displaying section

Result section

| | | Green cell: Required |
| Yellow cell: Editable |
| Gray cell: Uneditable |

3-2, Details of each sections

Condition setting up section

Circuit and criteria
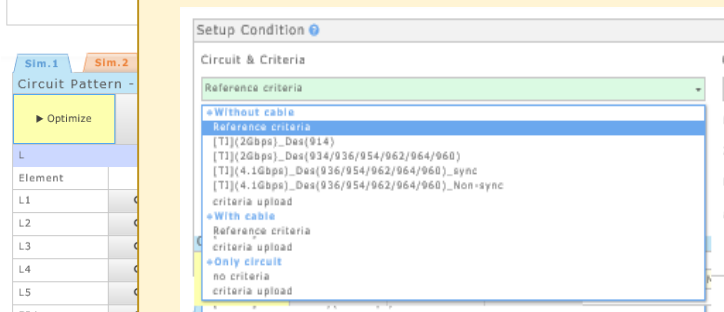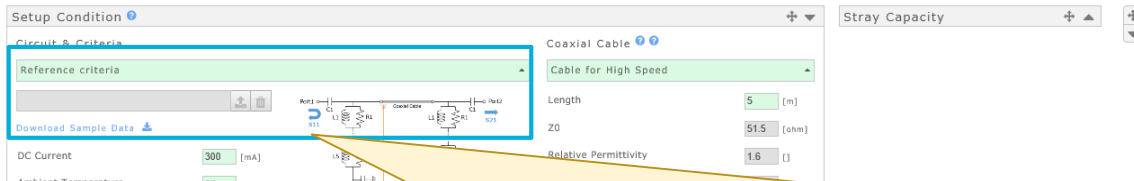
Circuits and criteria can be selected from the pull-down menu

◆ **Selectable circuit**
- With cable
- Without cable
- Only circuit
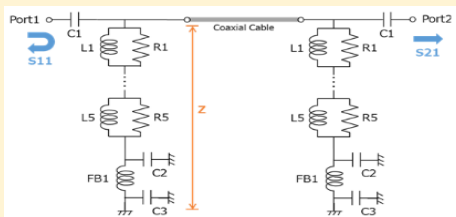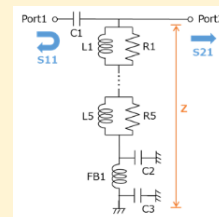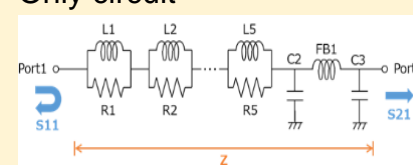
◆ **Selectable criteria**

- The IC manufacturer recommended criteria

- The criteria set by MURATA
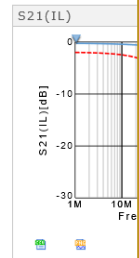
- Upload your criteria

3-2, Details of each sections

Condition setting up section

Current and Ambient temperature, cable conditions
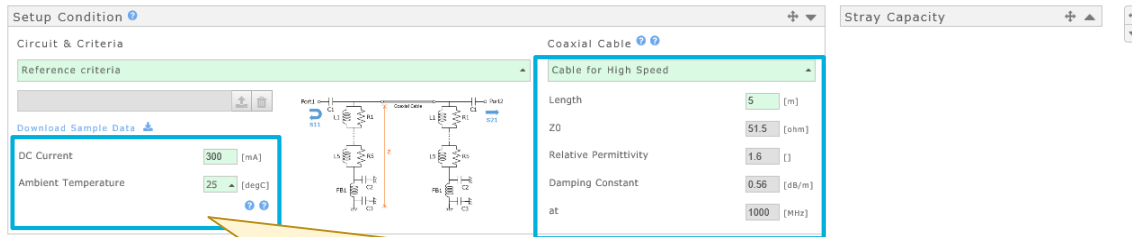
<- Input a rated current value required for parts

<- Select Ambient temperature

(selectable from 25, 85, 105, 115, 125°C)

In case selected "with cable " as the circuit
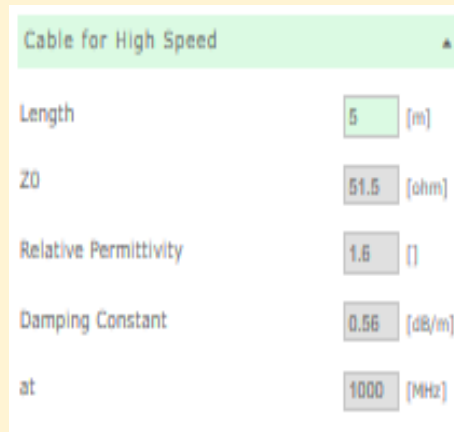
< Select cable (High speed:Max20GHz、Low speed:Max8.5GHz)

< Input cable length

Cable factor (editing available if "Edit" is selected in cable selection)

・Z0: Characteristic impedance

・ Relative permittivity: Cable permittivity

・Damping constant: Cable loss
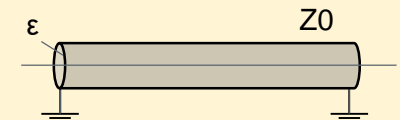
Damping constant

3-2, Details of each sections

Each elements setting and selected part number displaying section

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Delete all selected items for Sim. 1 to 5

Copy selected item

Paste copied item

Delete selected item

Set height limit of the filter consisting product

Perform automatic selection of optimal part number combinations

Optimization method
  -Maximize Margin :
   Find the part numbers combination that provides the best characteristics
  -Minimize Size :
   Find a combination of parts numbers with the smallest size that meets the criteria.

3-2, Details of each sections

Each elements setting and selected part number displaying section

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| Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5 | | | | | | Delete All Selected Partnumber |

Circuit Pattern - Sim.1

| ► Optimize | ✖ Delete | 🗐 Copy | 🗋 Paste | Optimization Method | Maximize Margin | Maximum Tsize | Free | [mm] |

L			Optimization Setup			R			C		
Element		P/N ❓		Status	Size Code	Element	Resistance ❓		Element	Capacitance ❓	
L1	🔍 Select	BLM18AG102SH1	✖	Optim.	Free	R1		[kohm]	C1	0.1	[uF]
L2	🔍 Select	LQW32FT100M0H	✖	Optim.	Free	R2	1.5	[kohm]	C2	0.1	[uF]
L3	🔍 Select	LQH3NPZ680MME	✖	Optim.	Free	R3	1.5	[kohm]	C3	0.01	[uF]
L4	🔍 Select		✖	None	Free	R4	1.5	[kohm]	-		
L5	🔍 Select		✖	None	Free	R5	1.5	[kohm]	-		
FB1	🔍 Select	BLM18KG102SH1	✖	Optim.	Free	-			-		

L1 - L5 : Part number that consist of the Bias-T filter
R1 - R5 : Parallel resistance
C1   : DC cut capacitor
C2, C3 : Decoupling capacitor
FB   : Ferrite Beads as a noise filter

With cable
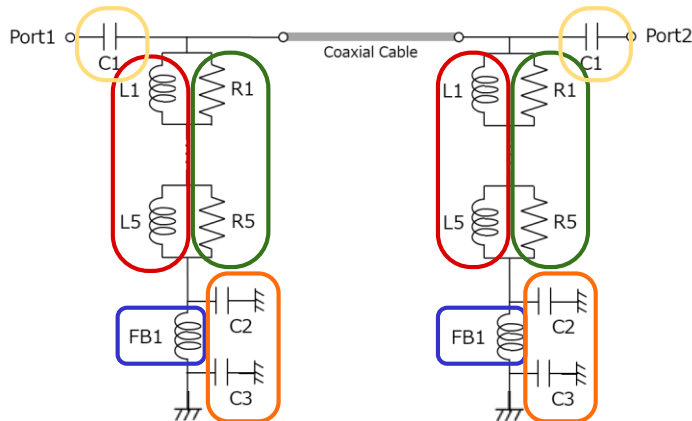
Without cable
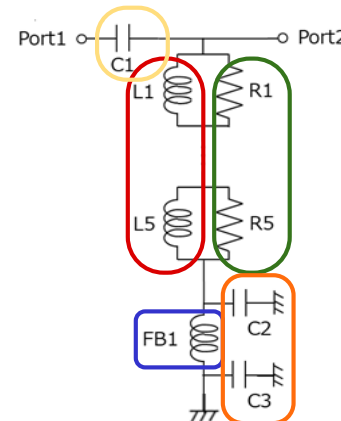
3-2, Details of each sections

Each elements setting and selected part number displaying section

Select Product

Display selected part number

Input parallel resistance value

Input capacitance value

Optimization setup
◎Status ⇒ Select the status of each elements
- Optim.: Automatically select the optimum product for this element by pressing the "Optimize" button.
- Fix. : Fix product even if the Optimize button is pressed
- None : Does not select automatically

◎Size code ⇒ Select the size of each elements.

3-2, Details of each sections

Result section

Export graph data as CSV

Total DC resistance value of selected part number(Max and typ.)

Display S21, S11, S21/S11, Z graphs

Total size and maximum height of selected part numbers

Minimum margin value against the criteria (Displaying markers in a graph)

Judgment (Pass/Fail) for criteria

Graph smoothing function

When "With cable" is selected, the influence of the reflection due to the cable is applied on the calculation result graph. The graph can be smoothed with the smoothing button.

List of selected part numbers and links

Like to selected art number
- Reference spec
- Product detail page
- SimSurfing (enables characteristic confirmation of single parts)

3-2, Details of each sections

Other features

	Move by section
	Open and close sections

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Use Case 1
(Automatic selection with "with cable" circuit)　1/2

PoC Bias-T filter design for ADAS cameras (With cable)
- Current　: 300 mA
- Ambient temperature : 105°C
- Cable length : 5 m
- Criteria : Reference criteria
Perform automatic selection

(1) Select With cable/Reference criteria as Circuit & Criteria

(3) Cable length: Input 5

(2) Current: Input 300, Temperature: Select 105°C

(4) Press the "Optimize" button

L						R			C			
Element		P/N	Status	Size Code		Element	Resistance		Element	Capacitance		
L1	Q Select	LQW18CNR47J0Z	Optim.	Free		R1	1.5	[kohm]	C1	0.1	[uF]	
L2	Q Select	LQW32FT470M0H	Optim.	Free		R2	1.5	[kohm]	C2	0.1	[uF]	
L3	Q Select	LQH3NPZ680MME	Optim.	Free		R3	1.5	[kohm]	C3	0.01	[uF]	
L4	Q Select		None	Free		R4	1.5	[kohm]	-			
L5	Q Select		None	Free		R5	1.5	[kohm]	-			
FB1	Q Select	BLM18KG102SH1	Optim.	Free		-			-			

Use Case 1
(Automatic selection with "with cable" circuit)　2/2

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L			Optimization Setup		R				C		
Element		P/N	Status		Element	Resistance			Element	Capacitance	
L1	Q Select	LQW18CNR47J0Z	x Optim.	Free	R1	1.5	[kohm]	▲	C1	0.1	[uF] ▲
L2	Q Select	LQW32FT470M0H	x Optim.	Free	R2	1.5	[kohm]	▲	C2	0.1	[uF] ▲
L3	Q Select	LQH3NPZ680MME	x Optim.	Free		1.5	[kohm]	▲	C3	0.01	[uF] ▲
L4	Q Select		x None	Free		1.5	[kohm]	▲	-		
L5	Q Select		x None	Free		1.5	[kohm]	▲	-		
FB1	Q Select	BLM18KG102SH1	x Optim.	Free					-		

(5) Results are displayed
In this case
**　　L1：LQW18CNR47J0Z**
**　　L2：LQW32FT470M0H**
**　　L3：LQH3NPZ680MME**
**　　FB：BLM18KG102SH1**
are automatically selected
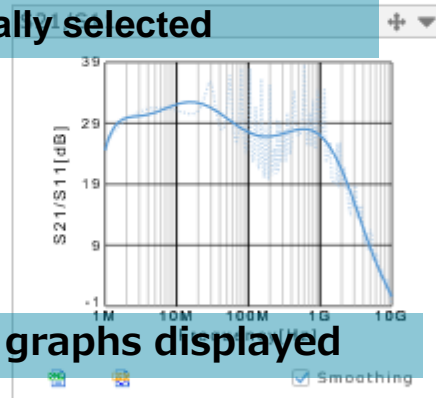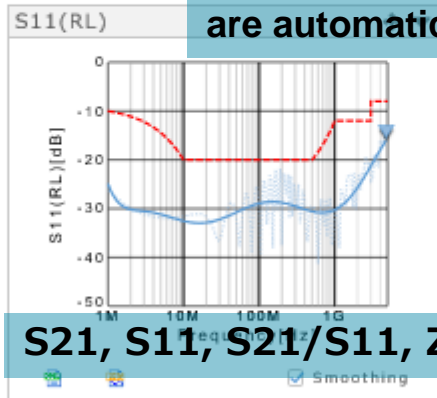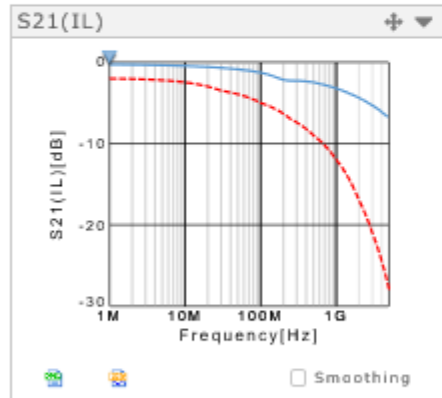
S21, S11, S21/S11, Z graphs displayed
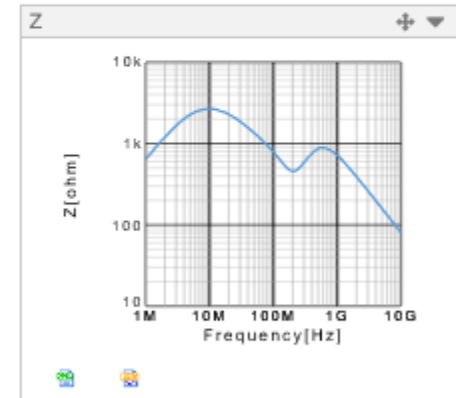
Result								
		Minimum Margin				Rdc		P/N
		S21[dB]	S11[dB]	S21/S11[dB]	Z[ohm]	Max.[ohm]	Typ.[ohm]	
Sim.1	**PASS**	1.73	7.51	-	-	2.93	2.47	📋 Selected Items

Chip Size	
Sim.1	Total [mm2] 19.56
	T Max.[mm] 2.50
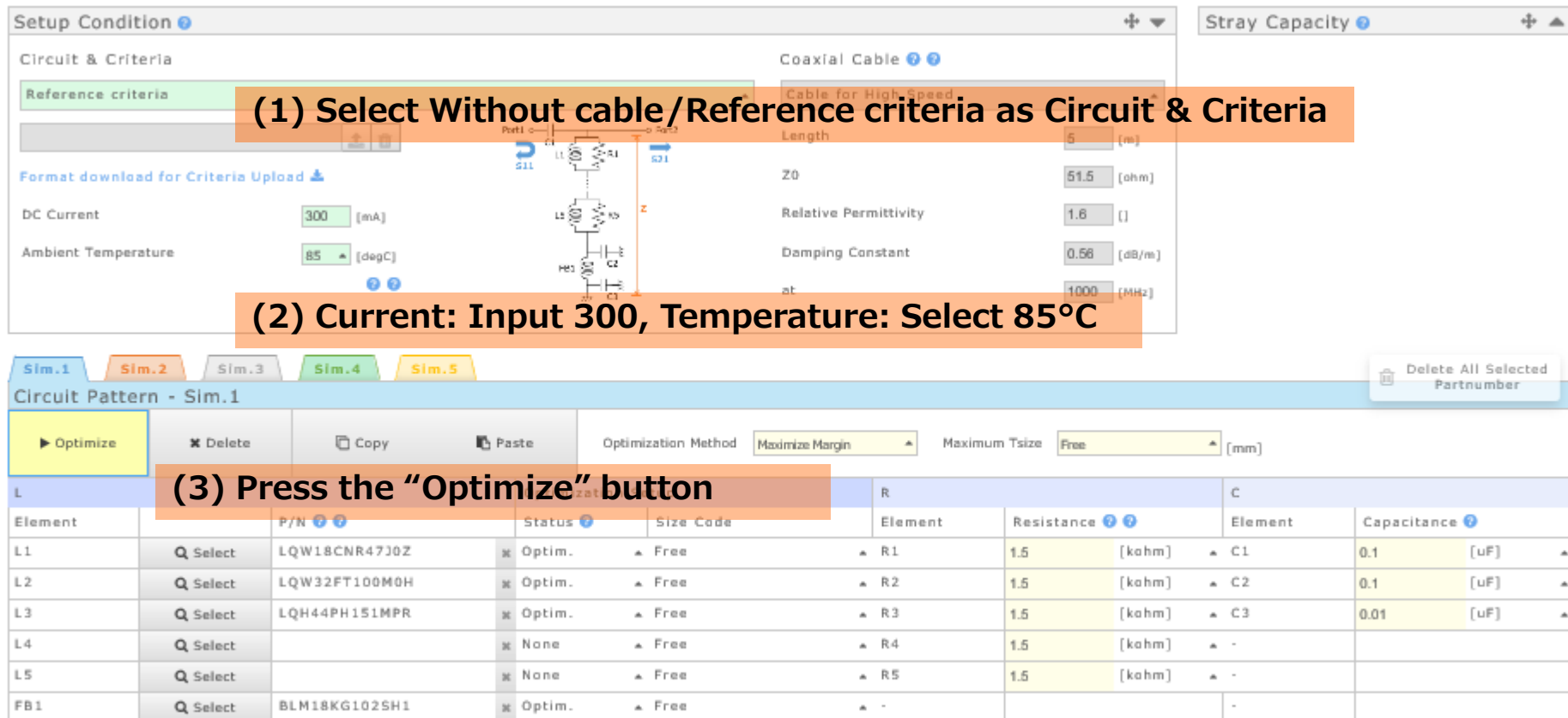
Pass or Fail against selected criteria, minimum margin value, total DCR, and total area are displayed

Use Case 2
(Automatic selection with "without cable" circuit)   1/2

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PoC Bias-T filter design for ADAS cameras (Without cable)
- Current : 300 mA
- Ambient temperature : 85°C
- Criteria : Reference criteria
Perform automatic selection

Setup Condition

Circuit & Criteria

Reference criteria

(1) Select Without cable /Reference criteria as Circuit & Criteria

Format download for Criteria Upload

DC Current   300 [mA]

Ambient Temperature   85 [degC]

(2) Current: Input 300, Temperature: Select 85°C

Coaxial Cable

Cable for High Speed

Length   5   [m]

Z0   51.5 [ohm]

Relative Permittivity   1.6   []

Damping Constant   0.56 [dB/m]

at   1000 [MHz]

Stray Capacity

| Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5 |

Circuit Pattern - Sim.1

| ▶ Optimize | ✘ Delete | 🗐 Copy | 🗐 Paste | Optimization Method | Maximize Margin | Maximum Tsize | Free | [mm] |

Delete All Selected Partnumber

(3) Press the "Optimize" button

L					R			C		
Element		P/N	Status	Size Code	Element	Resistance		Element	Capacitance	
L1	Q Select	LQW18CNR47J0Z	✗ Optim.	▲ Free	R1	1.5	[kohm]	C1	0.1	[uF]
L2	Q Select	LQW32FT100M0H	✗ Optim.	▲ Free	R2	1.5	[kohm]	C2	0.1	[uF]
L3	Q Select	LQH44PH151MPR	✗ Optim.	▲ Free	R3	1.5	[kohm]	C3	0.01	[uF]
L4	Q Select		✗ None	▲ Free	R4	1.5	[kohm]	-		
L5	Q Select		✗ None	▲ Free	R5	1.5	[kohm]	-		
FB1	Q Select	BLM18KG102SH1	✗ Optim.	▲ Free	-			-		

https://ds.murata.co.jp/bist/?lcid=en-us

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(4) Results are displayed
In this case
        L1 : LQW18CNR47J0Z
        L2 : LQW32FT100M0H
        L3 : LQH44PH151HPR
        FB : BLM18KG102SH1
are automatically selected

S21, S11, S21/S11, Z graphs displayed

Pass or Fail against selected criteria, minimum margin value, total DCR, and total area are displayed

Use Case 3
(Change optimization method and Compare) 1/2

https://ds.murata.co.jp/bist/?lcid=en-us

PoC Bias-T filter design for ADAS cameras (with cable)
- Current :500 mA
- Ambient temperature : 105°C
- Cable length : 10 m
- Criteria : Reference criteria
Compare the results when "maximum margin" and "minimum size" are selected as the "Optimization method "

(1) Select With cable/Reference criteria as Circuit & Criteria

(3) Cable length: Input 10

(2) Current: Input 500, Temperature: Select 105°C

*A message is displayed if the current value before input is smaller than 500 mA. Select the "Delete items that do not meet the condition" option and then click OK.

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Use Case 3
(Change optimization method and Compare) 2/2

**(4) Click the Optimize button with
Sim1 Optimization method: Maximize margin
Sim2 Optimization method: Minimize size**

**(5) Results are displayed
In this case
For "Maximize margin"
    L1 : LQW18CNR21J0Z
    L2 : LQW32FT220M0H
    L3 : LQH44PH330MPR
For "Minimize size"
    L1 : BLM18EG181SH1
    L2 : LQW18CNR27J0Z
    L3 : LQW32FT220M0H
    are automatically selected**

**Graphs, margin values, size images, total DCR
values, and total size values can be compared**

Use Case 4
(Reselect L from inductor list) 1/3

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PoC Bias-T filter design for ADAS cameras (without cable)
- Current : 400mA
- Ambient temperature :105℃
- Criteria : Reference Criteria
Reselect the L1 element after automatic selection and compare.

Setup Condition

Circuit & Criteria

Reference criteria

Format download for Criteria Upload

DC Current: 400 [mA]

Ambient Temperature: 105 [degC]

Coaxial Cable

Length: 5 [m]

Z0: 51.5 [ohm]

Relative Permittivity: 1.6 []

Damping Constant: 0.56 [dB/m]

Stray Capacity

(1) Select Without cable／Reference criteria as Circuit & Criteria

(2) Current: Input 500, Temperature: Select 105°C

| Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5 |

Circuit Pattern - Sim.1

▶ Optimize ✖ Delete 📋 Copy 📋 Paste   Optimization Method Maximi...

🗑 Delete All Selected Partnumber

(4) Results are displayed In this case For "Maximize margin"
   L1 : LQW18CNR39J0Z
   L2 : LQW32FT4R7M0H
   L3 : LQH44PH330MPR
are selected

(3) Press the "Optimize" button

Element		P/N	Status	Size Code					Capacitance
L1	Q Select	LQW18CNR39J0Z	✖ Optim.	▲ Free					0.1 [uF]
L2	Q Select	LQW32FT4R7M0H	✖ Optim.	▲ Free					0.1 [uF]
L3	Q Select	LQH44PH330MPR	✖ Optim.	▲ Free				C3	0.01 [uF]
L4	Q Select		✖ None	▲ Free					
L5	Q Select		✖ None	▲ Free		▲ R5	1.5 [kohm]	▲ -	
FB1	Q Select	BLM18KG102SH1	✖ Optim.	▲ Free		▲ -			

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(5) Copy product names selected in "Sim1"

(6) Select "Sim2"

(7) Attach the Sim1 part number by clicking Paste

(8) Click "Select" of L1

(9) Select an inductor

Change
LQW18CNR39J0Z to
BLM18HE152SH1

Use Case 4
(Reselect L from inductor list)　3/3

S21(IL)	⊹ ▾

S11(RL)	⊹ ▾

S21/S11	⊹ ▾

Z	⊹ ▾

☐ Smoothing ☑ Smoothing ☑ Smoothing

Result ⊹ ▾

		Minimum Margin				Rdc		P/N
		S21[dB]	S11[dB]	S21/S11[dB]	Z[ohm]	Max.[ohm]	Typ.[ohm]	
Sim.1	PASS	0.11	7.75	-	-	1.31	1.09	🗋 Selected Items
Sim.2	PASS	0.07	6.31	-	-	1.53	1.26	🗋 Selected Items
Sim.3	NA	-	-	-	-	-	-	🗋 Selected Items
Sim.4	NA	-	-	-	-	-	-	🗋 Selected Items
Sim.5	NA	-	-	-	-	-	-	🗋 Selected Items

Chip Size ⊹ ▾

	Total [mm2]	T Max.[mm]
Sim.1	26.56	2.50
Sim.2	26.56	2.50
Sim.3	-	-

(10) Results are displayed
Comparison of results when
LQW18CNR39J0Z or BLM18HE152SH1
is used for L1

Use Case 5
(Relax the set up condition after the result become "Fail") 1/3

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PoC Bias-T filter design for ADAS cameras (With cable)
- Current : 400 mA
- Ambient temperature : 125°C
- Cable length : 15 m
- Criteria : Reference criteria
Relax the set up condition after the result become "Fail"

Setup Condition

Circuit & Criteria

Reference criteria

(1) Select With cable/Reference criteria as Circuit & Criteria

Download Sample Data

DC Current   400 [mA]

Ambient Temperature   125 ▲ [degC]

Stray Capacity

Coaxial Cable

Length   15   [m]

Z0   51.5 [ohm]

(3) Cable length: Input 15

Relative Permittivity   1.6 []

Damping Constant   0.56 [dB/m]

at   1000 [MHz]

(2) Current: Input 400, Temperature: Select 125°C

Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5

Circuit Pattern - Sim.1

▶ Optimize | ✖ Delete | 🗐 Copy | 📋 Paste | Optimization Method Maximize Margin ▲ | Maximum Tsize Free ▲ [mm]

Partnumber

(4) Press the "Optimize" button

Result

Chip Size

(5) Result become "Fail"
In this case, since the temperature condition is 125 ° C and the cable length is 15 m, the condition is severe, so there is no combination that passes the criteria.

Rdc   P/N

Sim.1

S21[dB]

Total [mm2] 5.12
T Max.[mm] 0.95

Selected Items

Sim.1 | FAIL | 0.70

Use Case 5
(Relax the set up condition after the result become "Fail") 2/3

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i , Relax the temperature condition (125℃->105℃)

DC Current	400 [mA]	
Ambient Temperature	105 [degC]	

Relative Permittivity	1.6 []
Damping Constant	0.56 [dB/m]
at	1000 [MHz]

(6) Relax the temperature from 125C to 105C

Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5

Circuit Pattern - Sim.1

▶ Optimize | ✖ Delete | 🗐 Copy | 📋 Paste | Optimization Method: Maximize Margin | Maximum Tsize: Free [mm]

Delete All Selected Partnumber

(7) Press the "Optimize" button

L				Optimization Setup		R		C		
Element		P/N		Status	Size Code	Element	Resistance	Element	Capacitance	
L1	🔍 Select	LQW18CNR33J0Z	✖	Optim.	Free	R1	1.5 [kohm]	C1	0.1 [uF]
L2	🔍 Select	LQW32FT220M0H	✖	Optim.	Free	R2	1.5 [kohm]	C2	0.1 [uF]
L3	🔍 Select	LQH44PH330MPR	✖	Optim.	Free	R3	1.5 [kohm]	C3	0.01 [uF]
L4	🔍 Select		✖	None	Free	R4	1.5 [kohm]	-	
L5	🔍 Select		✖	None	Free	R5	1.5 [kohm]	-	
FB1	🔍 Select	BLM18KG102SH1	✖	Optim				-	

(8)Results are displayed
In this case
L1: LQW18CNR33J0Z
L2: LQW32FT220M0H
L3: LQH44PH330MPR
FB1 : BLM18KG102SH1
Are selected by relaxing
temperature condition and
pass the criteria.
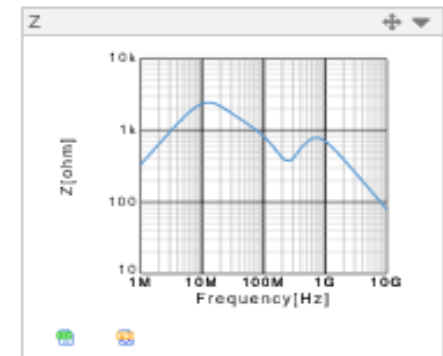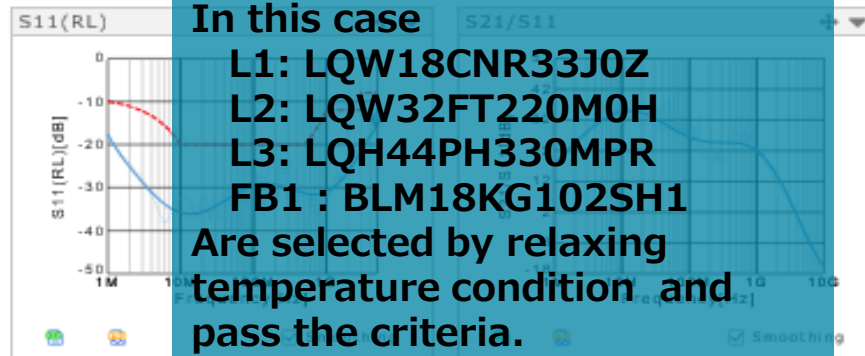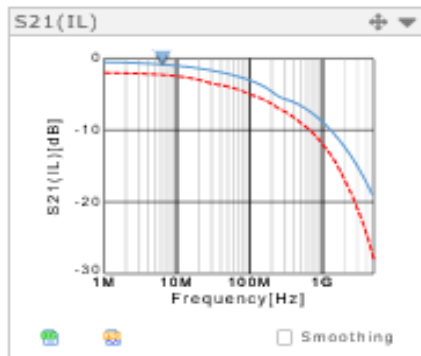
S21(IL) | S11(RL) | S21/S11 | Z

Result			Minimum Margin				Rdc		P/N
		S21[dB]	S11[dB]	S21/S11[dB]	Z[ohm]	Max.[ohm]	Typ.[ohm]	
Sim.1	PASS	1.44	7.42	-	-	1.62	1.37	📅 Selected Items

Chip Size | Sim.1 | Total [mm2] 26.56 | T Max.[mm] 2.50

Use Case 5
(Relax the set up condition after the result become "Fail") 3/3

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ii , Relax the temperature condition (125℃->105℃)+add element in series

DC Current 400 [mA]
Ambient Temperature 115 [degC]
Relative Permittivity 1.6 []
Damping Constant 0.56 [dB/m]
1000 [MHz]

(6) Relax the temperature from 125C to 115C
(There is no combination that pass the
criteria just by relaxing at 115 ℃.)

Sim.1 | Sim.2 | Sim.3 | Sim.4 | Sim.5

Circuit Pattern - Sim.2

Delete All Selected Partnumber

▶ Optimize | ✖ Delete | 🗋 Copy | 📋 Paste | Optimization Method: Minimize Size | Maximum Tsize: Free [mm]

(8) Press the "Optimize" button

L		P/N		Status	Size Code	R	Resistance	C	Element	Capacitance
Element						Element				
L1	Q Select	BLM18HE152SH1	✖	Optim.	Free	R1	1.5 [kohm]	C1	0.1	[uF]
L2	Q Select	LQW32FT100M0H	✖	Optim.	Free	R2	1.5 [kohm]	C2	0.1	[uF]
L3	Q Select	LQM21PH2R2NGC	✖	Optim.	Free	R3	1.5 [kohm]	C3	0.01	[uF]
L4	Q Select	LQW32FT100M0H	✖	Optim.	Free					
L5	Q Select		✖	None			1.5 [kohm]			
FB1	Q Select	BLM18KG102SH1	✖	Optim.	Free					

(7)Select "Optim." as L4 status
(Series elements number become 4pcs)

S21(IL) | S11(RL) | S21/S11 | Z

(8)Results are displayed
In this case
    L1: BLM18HE152SH1
    L2: LQW32FT100M0H
    L3: LQM21PH2R2NGC
    L4 : LQW32FT100M0H
Are selected by relaxing
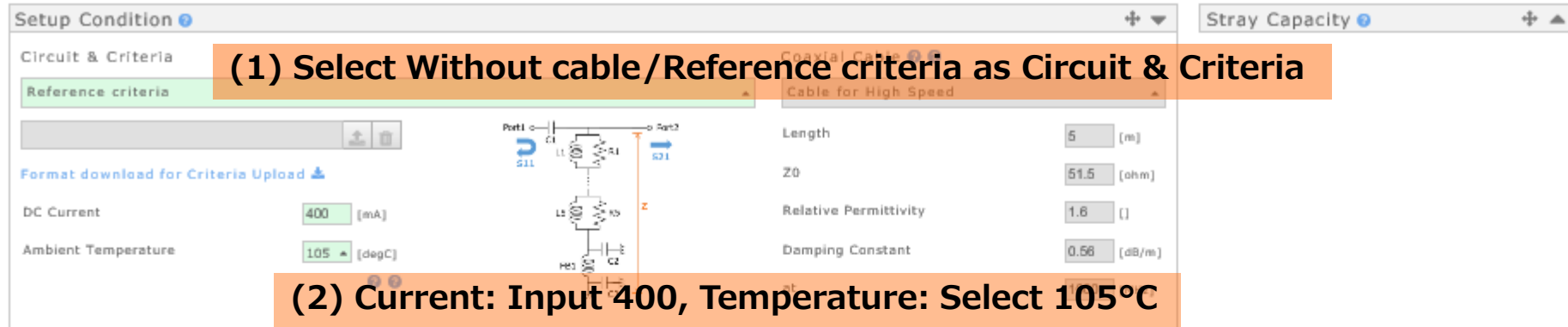**temperature condition and**
pass the criteria

Result		Minimum Margin						
		S21[dB]	S11[dB]	S21/S11[dB]	Z[ohm]	Max.[ohm]		Total [mm2] 18.56 T Max.[mm] 2.50
Sim.1	FAIL	-0.01	3.43	-	-	1.50		
Sim.2	PASS	0.02	4.93	-	-	1.7		Total [mm2] 20.96 T Max.[mm] 2.50
Sim.3	NA	-	-	-	-	-		

Use Case 6 (Reduce parallel R) 1/2

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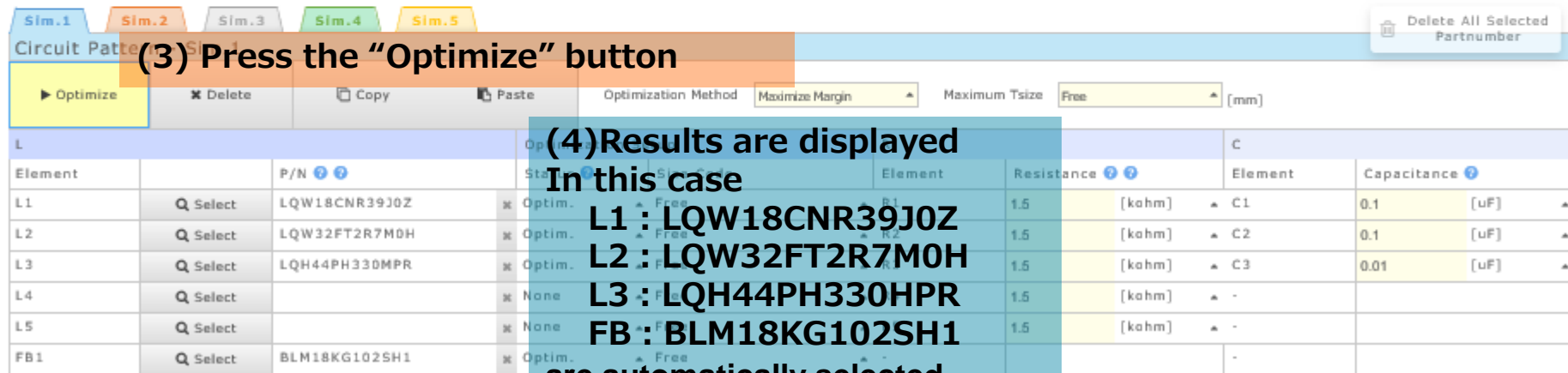PoC Bias-T filter design for ADAS cameras (Without cable)
- Current　: 400 mA
- Ambient temperature : 105°C
- Criteria : Reference criteria
Reduce parallel R

(1) Select Without cable/Reference criteria as Circuit & Criteria

(2) Current: Input 400, Temperature: Select 105°C

(3) Press the "Optimize" button

**(4)Results are displayed
In this case
L1 : LQW18CNR39J0Z
L2 : LQW32FT2R7M0H
L3 : LQH44PH330HPR
FB : BLM18KG102SH1
are automatically selected**

Use Case 6 (Reduce parallel R) 2/2

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End